CLAIMS

1. An apparatus comprising:

one or more logic circuits configured to provide computation, wherein said one or more logic circuits comprise dedicated logic within a programmable logic device (PLD).

2. The apparatus according to claim 1, wherein said one or more logic circuits comprise variable width logic circuits.

3. The apparatus according to claim 2, wherein a width of each of said one or more logic circuits is determined in response to one or more input signals.

4. The apparatus according to claim 1, wherein each of said one or more logic circuits is configured to receive a first one or more inputs, wherein said first one or more inputs comprise multi-bit or single-bit signals in a serial or a parallel configuration.

5. The apparatus according to claim 1, wherein each of said one or more logic circuits comprises a hard wired multiplier.

6. The apparatus according to claim 1, wherein said one or more logic circuits are configured to perform a cyclic redundancy check (CRC) functions.

7. The apparatus according to claim 1, wherein each of said one or more logic circuits is configured to present an output.

8. The apparatus according to claim 7, wherein each of said one or more outputs comprise partial product signals.

9. The apparatus according to claim 7, further comprising:

an adder circuit configured to receive said one or more outputs.

10. The apparatus according to claim 9, further comprising a routable interconnect circuit.

11. The apparatus according to claim 11, further comprising a number of registers configured to increase a throughput of said one or more logic circuits.

12. The apparatus according to claim 1, wherein each of said one or more logic circuits comprise an input portion configured to store one or more input signals.

13. The apparatus according to claim 12, wherein each of said one or more logic circuits comprises an output portion configured to store an output.

14. The apparatus according to claim 1, wherein each of said one or more logic circuits comprises an I/O portion configured to store a value.

15. An apparatus comprising:

means for receiving one or more input signals; and

means for computing comprising dedicated logic within a programmable logic device (PLD).

16. A method for computing in a Programmable Logic Device comprising the steps of:

(A) receiving one or more input signals; and

(B) computing with dedicated logic within said programmable logic device (PLD).

17. The method according to claim 16, further comprising the step of:

(C) generating one or more partial product signals.

18. The method according to claim 17, wherein step (C) further comprises:

multiplying said one or more input signals.

19. The method according to claim 16, wherein step (B) further comprises:

receiving said one or more outputs and adding said one or more outputs.

20. The method according to claim 16, wherein step (B) further comprises:

routing said one or more outputs.

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